

HOLE TOLERANCE  
UNLESS SPECIFIED  
PLATED: +/- .003  
NON PLATED: +/- .002


FINISHED HOLES IN MILS				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	PLATED	QTY	TOLERANCE/NOTES
•	5.0	PLATED	8	DIA MAX
•	10.0	PLATED	1190	DIA MAX
◦	15.0	PLATED	7	
◦	25.0	PLATED	1	
△	40.0	PLATED	56	
◦	45.0	PLATED	38	
◦	50.0	PLATED	2	
◦	60.0	PLATED	2	
□	65.0	PLATED	2	
A	50.0	NON-PLATED	1	
B	125.0	NON-PLATED	4	

TOTAL HOLES: 1311

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	04AUG23	E. REYTA
B	ECR-116884	19DEC23	E. REYTA
B1	ECR-119050(UPDATE DNI LIST ON ASSY NOTES ONLY) (NO CHANGE ON LAYOUT)	29JAN24	E. REYTA

TENTED VIA  
TENTED VIA

PRIMARY SIDE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES			APPROVAL		DATE		<div><div></div><div>ANALOG DEVICES</div></div> <div>WWM DIVISION 804 WOBURN STREET WILMINGTON, MA 01887</div>			
TOLERANCES			TEMPLATE ENGINEER BILLY PHILLIPS		07APR21					
DECIMALS   FRACTIONS   ANGLES			HARDWARE SERVICES BOB MACDONALD		07APR21					
.XX   -.010   --1/32   -- 2 .XXX   -.005 .XXXX   -.0050			HARDWARE SYSTEMS DAVE WILLIAMS		07APR21					
MATERIAL			TEST ENGINEER N/A		N/A		TITLE  FABRICATION  MAX32670-LR-ARDZ			
			COMPONENT ENGINEER ADGT LIBRARY		04AUG23					
			TEST PROCESS N/A		N/A					
			HARDWARE RELEASE C. PASIA		19DEC23					
FINISH			DESIGNER C. PASIA		19DEC23		SIZE	FSCM NO	DRAWING NUMBER	REV
			PTD ENGINEER E. REYTA		19DEC23					
			CHECKER N/A		N/A					
DO NOT SCALE DWG							SCALE	1 / 1		SHEET   1 OF 2

D

- C

## B

- A

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17. FINAL ELECTRICAL TEST TO BE PERFORMED USING PROVIDED IPC-D-356A NETLIST OR ODB++ FORMAT FILE. THE PCB SHALL HAVE A VERIFICATION STAMP.
18. A TIME DOMAIN REFLECTOMETER REPORT (TDR) FOR EACH IMPEDANCE CONTROLLED LAYER & A CERTIFICATE OF COMPLIANCE SHALL BE PROVIDED BY VENDOR AT TIME OF SHIPMENT. INSTANCES WHERE TDR TESTING CAN'T BE PERFORMED BECAUSE THE TRACE LENGTH IS TOO SHORT ON THE OUTER LAYERS AT THE PIN ESCAPES IS ACCEPTABLE. ALL OTHER INSTANCES MUST BE REPORTED.

19. IF PRESENT, ALL BLIND/BURIED VIAS WITH AN ASPECT RATIO  $<1:1$  TO BE PLATED SHUT WITH COPPER WHEN USED AS VIA-IN-PAD OR AS A STACKED VIA. BLIND/BURIED VIAS WITH AN ASPECT RATIO  $>1:1$  TO BE FILLED WITH NON-CONDUCTIVE EPOXY.
20. FOR VIA FILL INFORMATION REFER TO DRILL CHART:
  - ( ) NON-CONDUCTIVE EPOXY FILL ALL 0.0050 INCHES AND 0.0100 INCHES DRILLED VIAS
  - ( ) COPPER FILL ALL 0.XXXX INCHES DRILLED VIAS
21. INTENTIONAL SHORTS:
  - IF AN INTENTIONAL SHORT REPORT IS SUPPLIED AND DOES NOT MATCH THE FAB DATA THEN ADI APPROVAL IS REQUIRED.
22. PENNUTS:
  - ( ) PENNUTS TO BE INSTALLED BY FABRICATOR
  - ( ) PENNUTS NOT TO BE INSTALLED BY FABRICATOR
  - (X) NOT APPLICABLE
23. MANUFACTURER TO ETCH/STAMP WITH PERMANENT NON-CONDUCTIVE INK ON SECONDARY SIDE UNLESS OTHERWISE SPECIFIED:
  - A. UL CODE-FLAMMABILITY RATING FOR THOSE APPROVED MATERIALS(IF APPLICABLE)
  - B. DATE CODE
  - C. LOT NUMBER
  - D. MANUFACTURER LOGO
24. MINIMUM DESIGN LINE WIDTH IS .006 INCH.
25. MINIMUM DESIGN LINE SPACING IS .004 INCH.
26. BOARDS TO BE SHIPPED SINGULATED AFTER FABRICATION PROCESS.  
SMOOTHEN EDGES AND FREE FROM BURRS AFTER DEPANELIZATION PROCESS

D

C

B

A

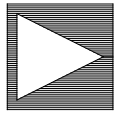
LAMINATION DIAGRAM				
LAYER NUMBER	LAYER NAME	FINISHED CU WEIGHT (OZ)	DIELECTRIC THICKNESS (INCH)	MATERIALS
1	TOP	1.5		FINAL CU (THICKNESS AFTER PLATING)
			0.0063	ISOLA 370HR/EQUIVALENT
2	L2_GND	1		CU CLAD
			0.044	ISOLA 370HR/EQUIVALENT
3	L3_PWR	1		CU CLAD
			0.0063	ISOLA 370HR/EQUIVALENT
4	BOTTOM	1.5		FINAL CU (THICKNESS AFTER PLATING)

THE FINISHED PCB THICKNESS TO BE: 0.062" +/-0.006"

PRIMARY SIDE

IMPEDANCE TABLE
IMPEDANCE TOLERANCE: +/-10%
CPWG IMPEDANCE( SPACE/TRACE/SPACE )
50 OHM ON TOP : 0.01200/0.01100/0.01200

NOTE: DO NOT EDIT THIS TABLE MANUALLY;USE IMPEDANCE TABLE GENERATOR FROM ADI Tools.



# ANALOG DEVICES

WWM  
DIVISION  
804 WOBURN STREET  
WILMINGTON, MA 01887

SIZE	FSCM NO	DRAWING NUMBER		REV
C	24355	09-079882		B
SCALE	1/1		SHEET 2 OF 2	